Amendments to the Claims

Claims 1-9 (*Cancelled*)

10. (*Cancelled*)

11. (*Currently Amended*) The processing system of ~~claim 10~~ claim 13,

wherein said device is further operable to store the first destination address as a default-destination-address as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first destination address in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

12. (*Cancelled*)

13. (*Currently Amended*) ~~The processing system of claim 12,~~ A processing system, comprising:

a device operable to decode a first program instruction into a first microcode instruction, said device further operable to decode a second program instruction into a second microcode instruction;

a circuit in electrical communication with said device, said circuit operable to process the first microcode instruction subsequent to a first decoding of the first program instruction by said device, said circuit further operable to process the second microcode instruction subsequent to a second decoding of the second program instruction by said device and a first processing of the first microcode instruction by said circuit;

wherein the first program instruction includes a first field defining a first jump type to be decoded by said device;

wherein the first program instruction further includes a second field defining a first destination address to be decoded by said device;

wherein the first program instruction further includes a fifth field defining a first jump condition to be decoded by said device;

wherein the second program instruction includes a third field defining a second jump type to be decoded by said device; and

wherein a fourth field defines a second destination address to be decoded by said device, and the second program instruction excludes the fourth field.

wherein a sixth field defines a second jump condition to be decoded by said device, and the second program instruction excludes the sixth field.

wherein said device is further operable to store the first jump condition as a default-condition as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device

14. (*Currently Amended*) The processing system of ~~claim 10,~~ claim 13,

wherein said device is further operable to decode a third program instruction into a third microcode instruction;

wherein said circuit is further operable to process the third microcode instruction subsequent to the first processing of the first microcode instruction by said circuit, prior to the second decoding of the second program instruction by said device and subsequent to a third decoding of the third program instruction by said device;

wherein the third program instruction includes a fifth field defining a first jump condition to be decoded by said device;

wherein a sixth field defines a second jump condition to be decoded by said device, and the second program instruction excludes the sixth field.

15. (*Previously Presented*) The processing system of claim 14,

wherein said device is further operable to store the first jump condition as a default-condition as a result of the third decoding of the third program instruction by said device; and

wherein said device is further operable to include the first jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

16. (*Currently Amended*) The processing system of ~~claim 10,~~ claim 13, wherein the first jump type is one of a branch instruction or a call instruction.

17. (*Currently Amended*) The processing system of ~~claim 10,~~ claim 13, wherein the second jump type is one of a branch instruction or a call instruction.

18. (*Cancelled*)

19. (*Currently Amended*) ~~The processing system of claim 18,~~ A processing system, comprising:

a device operable to decode a first program instruction into a first microcode instruction, said device further operable to decode a second program instruction into a second microcode instruction;

a circuit in electrical communication with said device, said circuit operable to process the first microcode instruction subsequent to a first decoding of the first program instruction by said device, said circuit further operable to process the second microcode instruction subsequent to a second decoding of the second program instruction by said device and a first processing of the first microcode instruction by said circuit;

wherein the first program instruction includes a first field defining a first jump type to be decoded by said device;

wherein the first program instruction further includes a second field defining a first jump condition to be decoded by said device;

wherein the second program instruction includes a third field defining a second jump type to be decoded by said device; and

wherein a fourth field defines a second jump condition to be decoded by said device, and the second program instruction excludes the fourth field;

wherein said device is further operable to store the first jump condition as a default-condition as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

20. (*Currently Amended*) The processing system of ~~claim 18,~~ claim 19, wherein the first jump type is one of a branch instruction or a call instruction.

21. (*Currently Amended*) The processing system of ~~claim 18,~~ claim 19, wherein the second jump type is one of a branch instruction or a call instruction.

22. (*Cancelled*)

23. (*Cancelled*)

24. (*Currently Amended*) ~~The processing system of claim 23~~, A processing system, comprising:

a device operable to decode a first program instruction into a first microcode instruction, said device further operable to decode a second program instruction into a second microcode instruction;

a circuit in electrical communication with said device, said circuit operable to process the first microcode instruction subsequent to a first decoding of the first program instruction by said device, said circuit further operable to process the second microcode instruction subsequent to a second decoding of the second program instruction by said device and a first processing of the first microcode instruction by said circuit;

wherein the first program instruction further includes a first field defining a first destination address to be decoded by said device;

wherein the second program instruction includes a second field defining a jump type to be decoded by said device; and

wherein the second program instruction excludes a fourth field defining a jump condition to be decoded by said device;

wherein a third field defines a second destination address to be decoded by said device, and the second program instruction excludes the third field; and

wherein said device is further operable to include the jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device; and

wherein said device is further operable to store the first destination address as a default-destination-address as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first destination address in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

25. (*Currently Amended*) The processing system of ~~claim 22,~~ claim 24, wherein the jump type is one of a branch instruction or a call instruction.

26. (*Cancelled*)

27. (*Currently Amended*) ~~The processing system of claim 26,~~ A processing system, comprising:

a device operable to decode a first program instruction into a first microcode instruction, said device further operable to decode a second program instruction into a second microcode instruction;

a circuit in electrical communication with said device, said circuit operable to process the first microcode instruction subsequent to a first decoding of the first program instruction by said device, said circuit further operable to process the second microcode instruction subsequent to a second decoding of the second program instruction by said device and a first processing of the first microcode instruction by said circuit;

wherein the first program instruction further includes a first field defining a first jump condition to be decoded by said device;

wherein the second program instruction includes a second field defining a jump type to be decoded by said device;

wherein said device is further operable to store the first jump condition as a default-condition as a result of the first decoding of the first program instruction by said device; and

wherein said device is further operable to include the first jump condition in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

28. (*Previously Presented*) The processing system of claim 27,

wherein the second program instruction excludes a fourth field defining a destination address to be decoded by said device; and

wherein said device is further operable to include the destination address in the second microcode instruction as a result of the second decoding of the second program instruction by said device.

29. (*Currently Amended*) The processing system of ~~claim 26;~~ claim 27,

wherein the jump type is one of a branch instruction or a call instruction.